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Electronic circuit implementation of the chaotic Rulkov neuron model

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Abstract

Numerical integration is the most common and straightforward approach in computational neuroscience for the study of biological neuron models based on ordinary differential equations. For some purposes, numerical simulations are not enough due to the multiple bottlenecks in computer architectures. However, when electronic circuits are used to simulate in real time large arrays of coupled neurons, the simulations are much faster than the computer simulations. We present here an electronic implementation of a map-based neuron model, a chaotic Rulkov neuron model, that can be easily transferred on a large scale integration circuit and thus provide a framework for the simulation of large networks of neurons. The Rulkov model is a map-based neuron model that has a surprising abundance of features, such as periodic and chaotic spiking and bursting. The discrete time dynamics allows to tune the time scale of the circuit to the needs of the specific application. Since the circuit described here only uses 18 MOS transistors, it offers new perspectives for building large networks of neurons in a single device. This is very relevant for the analysis of large networks of coupled neurons in order to investigate its dynamics over the network and its synchronization properties.

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1. Introduction

Many interesting properties arise when we consider interconnected dynamical systems. An important issue in this context is the way the dynamical systems are coupled. Different topologies of interconnectivity might be considered, giving rise to different dynamical

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global properties. The relevance of all these concepts appears when studying the phenomenon of synchronization. In particular when we consider networks of interconnected neurons, the analysis of the synchronization has received much attention in the past few years. An interesting review on the impact of Nonlinear Science in Biology appears in [1].

Synchronization of neuronal activity has been intensively studied as a collective behavior with possible relations with information transmission and processing in biological neurons. In these studies, ordinary differential equation (ODE) of neuron models with fast–slow dynamics is most commonly used. Nevertheless, map-based neuron models [2,3,6,8] have recently received much attention as reasonable units for simulating collective behaviors in large-scale neural networks. The reason is that map-based models have been found to be comparable to ODE models in reproducing characteristic behaviors of biological neurons [4,5,7].

A major challenge for engineers and scientists is to produce efficient tools to address the growing needs in computational power for the simulation of networks of coupled neurons. Devices that compute large networks in real time would be an asset for the field of computational neuroscience. For example, the study of the synchronization of arrays of neurons would be quickened a great deal when simulated with electronic circuits, allowing more time to analyze and produce data.

An artificial electronic neuron reproduces the observed behaviors of the real neurons by an emulation of the dynamics with the use of electronic circuits [9–11]. The mathematical models that have been built from neurophysiological data obtained in experiments are implemented in an electronic circuit simulating and reproducing its behavior. There exist a large number of models with higher or lower degrees of approximations to the observed neuronal dynamics. Given a particular problem, the choice of the model must be motivated by the relevant aspects of the dynamics, but also by the computational trade-offs. For example, a large number of continuous neuron models, benefit the accuracy of the model at the cost of its computational efficiency. This implies that a balance between these two design constraints must be taken into account at the time of the choice of the model equations.

We focus here on a class of models that combine two key elements for the study of large group of neurons: a simple modelling and a discrete time dynamics. The chaotic Rulkov map-based neuron model [3] is a good candidate to simulate large arrays of coupled neurons, since its dynamical properties are sound and its implementation in an electronic circuit is efficient.

There have been several efforts recently to implement versatile mathematical neuron models in silicon [12–14] that can exhibit a variety of behaviors by tuning the parameters. These implementations can be opposed to a precise reproduction of a physiological model [15] which relies on experimental observations of neurons. Most of the implementations of silicon neurons are built based on continuous time models [2,12] or on simpler discrete time models [13]. The discrete time dynamics has a series of interesting features when compared to continuous dynamical systems. First, the discrete process of iteration is a very well defined and simple mechanism using sample and hold blocks. Another interesting point is that the time scale of the simulation can be adapted in real time. The simulation rate can be chosen by changing the clock speed of the system and consequently the speed of the iteration process is regulated. This is of the most importance when we are interested in a very fast simulation.

On the other hand, the chaotic Rulkov model displays several neuron-like behaviors depending on the model parameters. Prior studies [2–4,7] have also shown that this model is a good alternative for the modeling of coupled neuron networks.

A VLSI (very-large-scale integration) architecture allows a parallel implementation and computation of the networks of neurons. The Complementary Metal Oxyde Semiconductor (CMOS) devices are a paradigmatic choice for this kind of applications for its affordable price and scalability. Although most of the CMOS designs nowadays are oriented to digital applications, they can be used as well for analog and mixed-signal circuits.

The main interest of implementing an electronic circuit of a map-based neuron that we describe in this paper aims at offering the key ingredient to build a large interconnected network which will be useful to analyze practical aspects in computational neuroscience like synchronization and interconnectivity.

2. Description of the electronic circuit

The chaotic Rulkov neuron model is an alternative to continuous time neuron models for the study of large interconnected networks. It has a simple and elegant formulation while keeping interesting dynamical regimes such as spiking and bursting [2,3]. The discrete time dynamics permits easy theoretical analysis with the profusion of tools available in nonlinear dynamics. The simulation of the model is also straightforward and very fast on modern computers since it involves only iterative loops. These features make this model an ideal candidate for simulations when the physiological details are not critical.

Even though the Rulkov map is an abstract mathematical model, it shares some specific features with other neuron models which are closer to experimental observations. The original chaotic Rulkov model as proposed in [3] can be expressed as a two dimensional discrete time model

$$x_{n+1} = \frac{\alpha}{1 + x_n^2} + y_n + I_n, \tag{1}$$

$$y_{n+1} = y_n - \sigma x_n - \beta. \tag{2}$$

The two variables of the model represent the two important time-scales of a neuron model: the fast dynamics of the system that holds for the membrane voltage of the neuron, and the slow variations of the ionic recovery currents. The variable x represents the fast dynamics whereas y is the slow dynamics. The variable I_n gathers the sum of the external influences on the neuron. Nonetheless, for convenience and without lack of generality, we will consider it to be always zero here.

These equations present a diversity of behaviors depending on the control parameters α and σ . The two typical regimes are the spiking regime: a series of short sustained pulses reminding the spike train of a neuron; and the bursting regime: a brief train of pulses alternating with a quiet state. An interesting point here is that chaotic trajectories exist in both regimes, which is due in part to the shape of the nonlinear function in Eq. (1).

This discrete map equation can be implemented in a circuit using two sample and hold (S/H) circuits for the iteration process of each variable as described in Ref. [16] for a one dimensional discrete time chaos generator. The simplified block diagram of the circuit can be seen in Fig. 1.

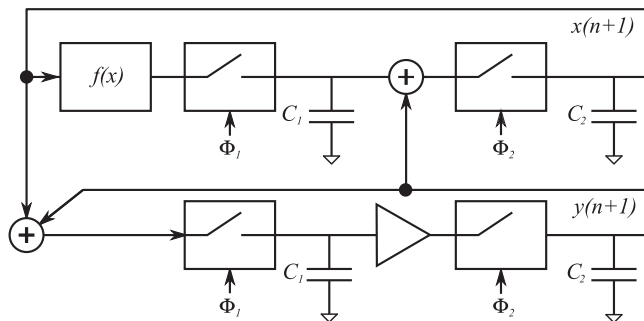


Fig. 1. Schematic electronic implementation of the Rulkov map neuron. The sample and hold blocks are controlled by the external clocks Φ_1 and Φ_2 . The nonlinear function f takes the value x_{n+1} as input and after its processing, the output value $f(x_{n+1})$ is obtained.

The two S/H circuits need clocks with the same frequency but with different phases. When a brief positive pulse is applied on Φ_1 , the input value of the block is transferred to the output and is stored into the capacitor C_1 as long as both switches are open. The impedance of the switches is considered infinite. Given a delayed pulse on Φ_2 on the gate of the second S/H circuit, the electric charge stored in C_1 is transferred and stored into the capacitor C_2 . The analog voltage held in this capacitor is the value of the iterate x_{n+1} (or y_{n+1}) that will be used to compute the next iteration. The delay between the two pulses is essential to perform the successive iterations of the map for each variable. The iteration is possible if only one of the switches is closed at once in order to keep the voltages of C_1 and C_2 independent. Additional buffers must be introduced in order to avoid charge injection and charge sharing between the S/H circuits that can affect the precision of the whole circuit. This charge injection is a major concern when dealing with S/H blocks as they reduce the voltage accuracy and consequently introduce errors in the sampling process. The buffers introduced in the design have the double objective to balance this effect and to sum up a voltage for the information processing. The sizes of the n -channel MOS (NMOS) transistors used for the switches are ($W/L = 0.4 \mu\text{m}/0.4 \mu\text{m}$) and all the capacitor values are $C = 1 \text{ pF}$.

Despite the simplicity of the model in Eqs. (1) and (2), a series of approximations and adaptations are needed for its implementation into a CMOS circuit. One of the most delicate points is the design of the nonlinear function

$$f(x_n) = \frac{\alpha}{1 + x_n^2}. \tag{3}$$

We propose an implementation of this function using the bump–antibump circuit [17]. It consists in a small circuit that takes advantage of the properties of the subthreshold region of the MOS transistors.

The DC transfer function of the circuit shown in Fig. 2(a) and (b) is a Gaussian shaped curve when a voltage input V_{in} is fed. The shape of the curve is similar enough to the nonlinear function in Eq. (3) for our purpose, which is mainly to obtain the same bifurcations in the phase plane. Two external bias voltages V_a, V_b allow to modify the shape and the properties of the function that have dramatic effects on the dynamics as we will show in detail in Section 3. The voltage V_a affects the horizontal position of the transfer function on the horizontal axis in Fig. 2(a) while V_b is related to the width of the

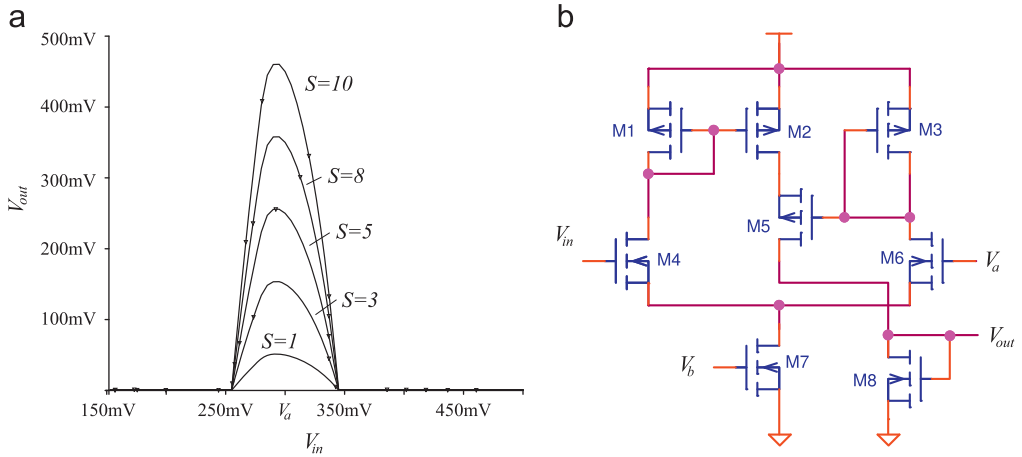


Fig. 2. This figure shows important characteristics of the electronic design of the function $f(x_n) = \alpha/(1 + x_n^2)$ of the model. (a) DC characteristics of the approximated function f for different values of the static gain S . (b) Schematics of the adapted bump circuit that implements the function f .

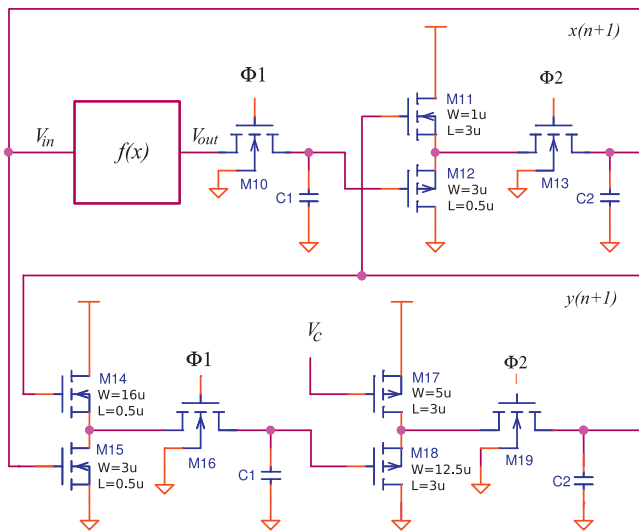


Fig. 3. Complete circuit of our approximated Rulkov model. The nonlinear function f is depicted in Fig. 2(b).

curve. The static gain S of the function can be tuned with the size factor (W/L) of the transistors.

With the following size (W/L) of transistors $M2 = M5 = (S \mu\text{m}/1 \mu\text{m})$ and $M1 = M3 = (6 \mu\text{m}/S \mu\text{m})$, the static gain of the transfer function increases with the parameter S as shown Fig. 2(a). The rest of the transistors have been sized as follows: $M4 = M6 = (15 \mu\text{m}/1 \mu\text{m})$, $M7 = (3 \mu\text{m}/1 \mu\text{m})$, $M8 = (1 \mu\text{m}/2 \mu\text{m})$. The circuit used in our design for the function f is shown in Fig. 2(b).

The block circuit representation of the circuit of the approximated Rulkov model can be seen in Fig. 3. Voltage followers are introduced between the S/H circuits in order to

prevent charge injection. Moreover, the transistor for bias adjustment of these followers can be used as a voltage adder when employed in the adequate linear region. These buffers are easily characterized by their DC transfer function which is a good approximation for the time discrete regime. The sub-circuit for the second variable y in the lower part of Fig. 3 consists also in two voltage followers with bias adjustment that implement the two necessary additions in Eq. (2). The first buffer, composed of the two NMOS transistors M14 and M15, performs the addition of σx_n and y_n , while the second buffer with the p -channel MOS (PMOS) transistors M17 and M18 adjust the constant β of Eq. (2) with the voltage V_c . The sizes of the transistors for the buffers are shown in Fig. 3. Another important adaptation is the scaling of the variables to get the dynamics of the circuit into an suitable regime. The dynamical range of the variables has been reduced and adapted to a single positive supply voltage of 5 V. The discrete equations of the system with these transformations can be approximated by

$$x_{n+1} = f(x_n) \cdot 0.8 + y_n + 0.2, \tag{4}$$

$$y_{n+1} = 1.1y_n - 0.25x_n + 0.62V_c. \tag{5}$$

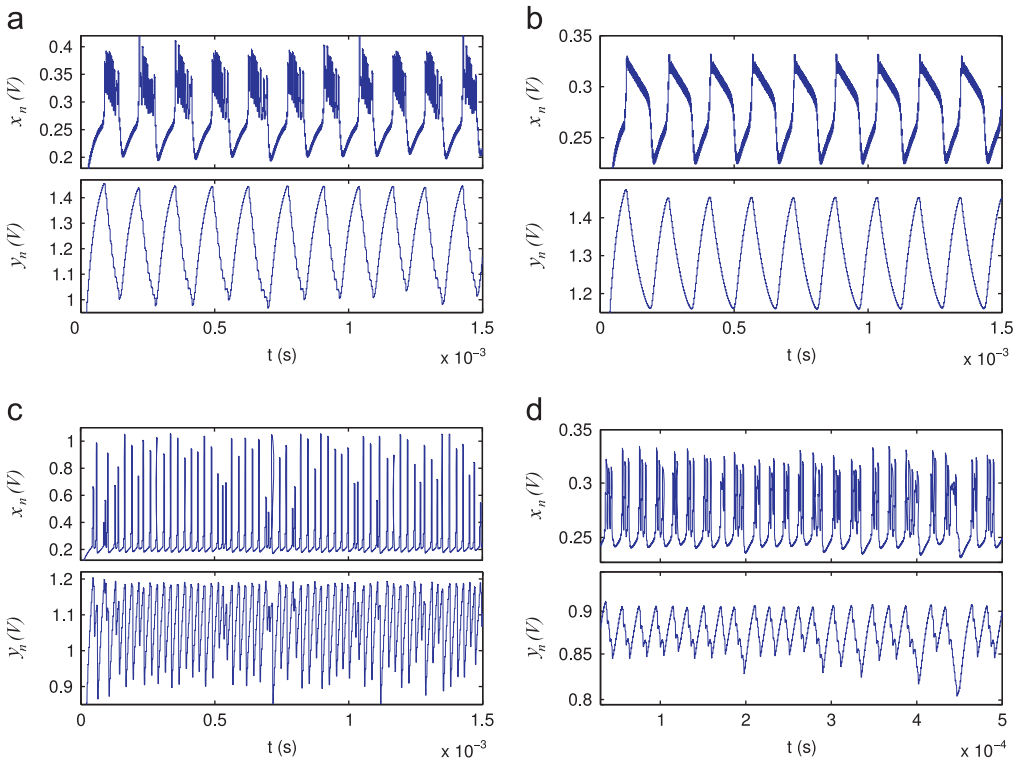


Fig. 4. This figure shows the time series of variables x and y of the circuit for some typical behavior of neuronal dynamics. (a) Typical chaotic burst behavior for $S=5$ and $V_b=0.3$ V. (b) Relaxation oscillations for $S=2$ and $V_b=0.3$ V. The amplitude of the oscillations is large in this case. (c) Chaotic spiking for $S=15$ and $V_b=0.35$ V. (d) Another chaotic bursting behavior for $S=3$, $V_a=0.28$ V and $V_b=0.075$ V. Notice that the time scale is different in this last case.

This is only an orientative approximation since the transistors will introduce additional nonlinearities in these equations.

3. Analysis and discussion of the results

We present the results of a Pspice simulation with a level 2 MOSFET transistor model. The time series of Fig. 4 have been simulated with a digital clock of frequency 1 MHz for the iteration process, producing a data rate of 1 MSps. The trajectory of the variable x in Fig. 4(a) shows the typical chaotic burst of the Rulkov model while the slow variable y switches the state of the variable x from chaotic oscillations to rest. Fig. 4(b) represents relaxation oscillations similar to the FitzHugh–Nagumo model as the system switches alternatively between two stable states. Fig. 4(c) depicts a case of chaotic spiking. Notice the fast dynamics of the variable y and the large amplitude which are a consequence of the large static gain $S=15$ of the function f . The bias voltages are $V_a=0.1$ V and $V_c=4.8$ V for these three examples. The last example in Fig. 4(d) shows a different case of chaotic bursting with a smaller amplitude but also with a faster time scale than the example of Fig. 4(a). The parameter V_a has been altered to $V_a=0.28$ V in this last example, showing its importance for the dynamical regime.

As mentioned earlier, the shape of the function f is essential to the dynamics of the model and can be tuned with three parameters: S , V_a and V_b . The parameter S depends on the size of the transistors and is therefore constant for a given circuit. The bias voltages V_a and V_b are the two accessible control parameters for the dynamical regime. They can be

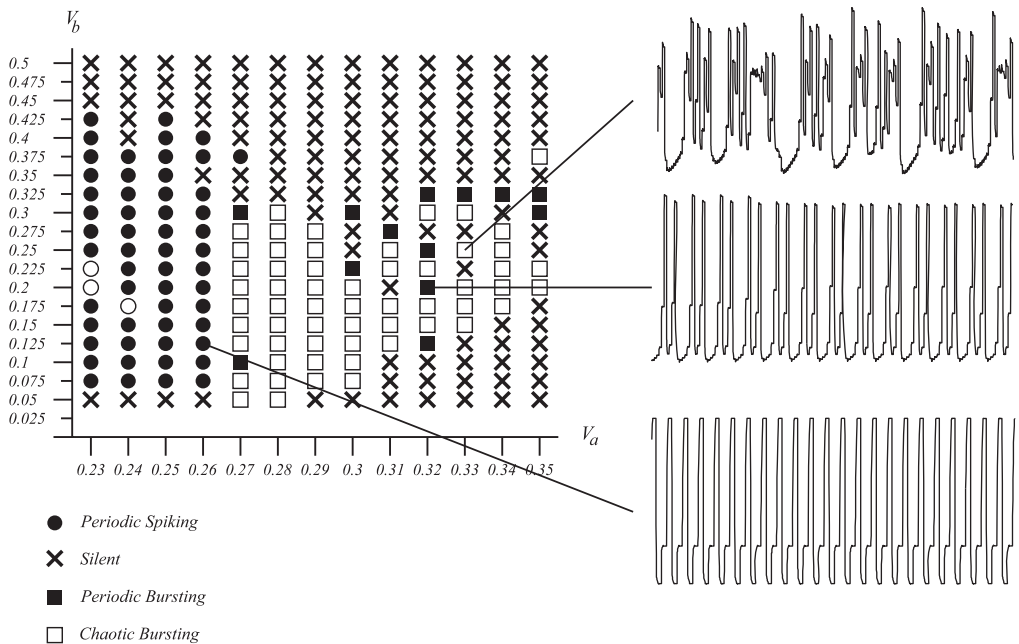


Fig. 5. Behavior of the circuit in function of the bias parameters V_a and V_b when $S=3$. Three different behaviors are accessible with a single parameter change. The time series in the insets are examples of chaotic and periodic bursting as well as autonomous oscillations that can be interpreted as periodic spiking.

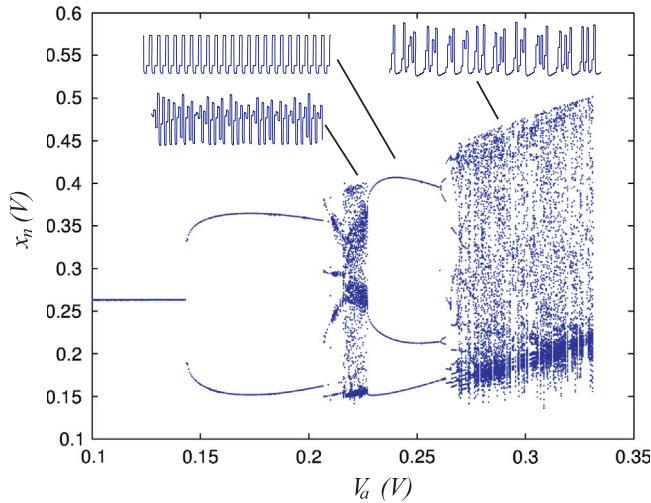


Fig. 6. Bifurcation diagram of the variable x in function of the parameter V_a for $V_b=0.25$ V and $S=3$. As V_a increases, the variable x exhibits first a silent behavior, and then periodic spiking finally chaotic bursting for $V_a > 0.27$ V. Notice the chaotic oscillations window around $V_a=0.23$ V.

adjusted at the time of the operation of the circuit but they may also evolve dynamically. The behavior of the model can be chosen from the diagram of Fig. 5, where the four most common types of oscillations are plotted in function of the parameters V_a and V_b . As these parameters change, so does the bifurcation structure of the artificial neuron in the phase plane $x-y$ leading to the different types of oscillation. Nevertheless, the bias voltage V_a alone can also be used as a single control parameter to tune the dynamical regime as shown in the bifurcation diagram of Fig. 6 for $V_b=0.25$ V. This diagram shows that chaotic as well as periodic oscillations are possible simply by varying the parameter V_a . The variable x exhibits first a silent behavior for values below $V_a=0.15$ V, then periodic spiking (period 2 and 3 windows) and finally chaotic bursting around $V_b=0.27$ V.

The simulations are reliable up to 1 MSps by changing the main clock frequency. The average power consumption of the circuit oscillates between 1 and 2 mW depending on the dynamical regime. This consumption can be however drastically reduced by introducing additional transistors that switch off the buffers when they are not in use. It is especially relevant at low frequencies when the circuit spends most of the time idle.

4. Conclusions

Current research projects aiming to study neuronal [18] dynamics are having increasing needs in computing power. The simulation of interconnected arrays of neurons is a demanding task for computers in terms of memory use and processing speed. As an alternative to the conventional computer architecture, we propose to perform these simulations with electronic circuits. As discussed in this paper, the chaotic Rulkov neuron model is an ideal candidate for an electronic circuit implementation. The main benefits of the electronic circuit implementation of the Rulkov neuron model can be summarized as follows. A wide range of possible dynamics can be chosen from the bifurcation diagrams of the electronic circuit depending of the needs of the application. With only one parameter

the dynamics can be changed from regular spiking to chaotic bursting. The speed of the simulations can be increased up to 1 million iterations per second by only changing the rate of an external clock. A major interest of these electronic circuits is their ability to work in parallel in a similar way to a living nervous system. The activity of a whole network can be monitored and observed in real time with a single device, whereas in classical computer architectures the simulation needs to finish before any possible analysis.

The approximated chaotic Rulkov neuron described in this paper offers the way to build a large interconnected networks composed of these units with the aim of analyzing practical aspects in computational neuroscience like modeling of cognitive processes, learning and behavior, synchronization, as well as applications to robotics or other technologies.

Acknowledgments

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References

- [1] A.V. Holden, Nonlinear science—the impact of biology, *Journal of the Franklin Institute* 334 (1997) 971–1014.
- [2] B. Ibarz, J.M. Casado, M.A.F. Sanjuán, Map-based models in neuronal dynamics, *Physics Reports* 501 (2011) 1–74.
- [3] N. Rulkov, Regularization of synchronized chaotic bursts, *Physical Review Letters* 86 (2001) 183–187.
- [4] G. Tanaka, B. Ibarz, M.A.F. Sanjuán, K. Aihara, Synchronization and propagation of bursts in a ring of coupled map neurons, *Chaos* 16 (2006) 013113.
- [5] B. Ibarz, G. Tanaka, M.A.F. Sanjuán, K. Aihara, Sensitivity versus resonance in two-dimensional spiking-bursting neuron models, *Physical Review E* 75 (2007) 041902.
- [6] B. Ibarz, J.M. Casado, M.A.F. Sanjuán, Patterns in inhibitory networks of simple map neurons, *Physical Review E* 75 (2007) 041911.
- [7] B. Ibarz, H. Cao, M.A.F. Sanjuán, Bursting regimes in map-based neuron models coupled through fast threshold modulation, *Physical Review E* 77 (2008) 051918.
- [8] J. Used, A. Wagemakers, M.A.F. Sanjuán, Regularization of map-based neuron models using phase control, *Discontinuity, Nonlinearity and Complexity I* (2012) 69–78.
- [9] A. Wagemakers, J.M. Casado, M.A.F. Sanjuán, K. Aihara, Building electronic bursters with the Morris–Lecar neuron model, *International Journal of Bifurcation and Chaos* 16 (2006) 3617–3630.
- [10] G. Indiveri, B. Linares-Barranco, T.J. Hamilton, A. van Schaik, R. Etienne-Cummings, T. Delbruck, S.C. Liu, P. Dudek, P. Häfliger, S. Renaud, J. Schemmel, G. Cauwenberghs, J. Arthur, K. Hynna, F. Folowosele, S. Saighi, T. Serrano-Gotarredona, J. Wijekoon, Y. Wang, K. Boahen, *Neuromorphic silicon neuron circuits*, *Frontiers in Neuroscience* 5 (2011) 1–23.
- [11] M.A. Mahowald, R. Douglas, A silicon neuron, *Nature* 354 (1991) 515–518.
- [12] N. Mizoguchi, Y. Nagamatsu, K. Aihara, T. Kohno, A two-variable silicon neuron circuit based on the Izhikevich model, *Artificial Life and Robotics* 16 (2011) 383–388.
- [13] M. Delgado-Restituto, A. Rodríguez-Vázquez, CMOS current-mode chaotic neurons, *IEEE International Symposium on Circuit and Systems* 6 (1994) 499–502.
- [14] J. Wijekoon, P. Dudek, Compact silicon neuron circuit with spiking and bursting behaviour, *Neural Networks* 21 (2008) 524–534.
- [15] A. Laffaquiere, S. Le Masson, J. Dom, G. Le Masson, Accurate analog VLSI model of calcium-dependent bursting neurons, in: *International Conference on Neural Networks*, vol. 2, 1997, pp. 882–887.
- [16] P. Dudek, V.D. Juncu, Compact discrete-time chaos generator circuit, *Electronics Letters* 39 (2003) 2–3.

- [17] T. Delbrück, Bump circuits for computing similarity and dissimilarity of analog voltages, in: IJCNN-91-Seattle International Joint Conference on Neural Networks, 1991, pp. 475–479.
- [18] J. Misra, I. Saha, Artificial neural networks in hardware: a survey of two decades of progress, *Neurocomputing* 74 (2010) 239–255.